

WHAT IS CLAIMED IS:

1. A power semiconductor device, comprising:
a first semiconductor layer of a first
conductivity type;

5 a second semiconductor layer of the first
conductivity type and a third semiconductor layer of a
second conductivity type which are alternately and
laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact
10 with the first semiconductor layer;

a fourth semiconductor layer of the second
conductivity type selectively formed in surface regions
of the second and third semiconductor layers;

a fifth semiconductor layer of the first
15 conductivity type selectively formed in a surface
region of the fourth semiconductor layer;

a second main electrode formed in contact with
surfaces of the fourth and fifth semiconductor layers;
and

20 a control electrode formed on surfaces of the
second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first
semiconductor layer is lower than that of the second
semiconductor layer; and a layer thickness ratio A is
25 given by an expression:

$$0 < A = t/(t+d) \leq 0.72$$

where t is a thickness of the first semiconductor layer,

and d is a thickness of the second semiconductor layer.

2. A semiconductor device according to claim 1,
wherein, assuming that an aspect ratio B is represented
by $B = d/w$, where w is an interval between adjacent
5 third semiconductor layers, the layer thickness ratio A
and the aspect ratio B satisfy an expression below:

$$A \times B \leq 1.15$$

3. A semiconductor device according to claim 1,
wherein an aspect ratio B and the layer thickness ratio
10 A satisfy an expression below:

$$- 0.04B + 0.48 < (A \times B) < 0.13B + 0.59$$

where the aspect ratio B is represented by $B = d/w$, and
w is an interval between adjacent third semiconductor
layers.

15 4. A semiconductor device according to claim 1,
wherein a product of $A \times B$ satisfies a relationship
below:

$$0.58 < (A \times B) < 0.71$$

wherein B denotes the an aspect ratio represented by B
20 $= d/w$, where w is an interval between adjacent third
semiconductor layers.

5. A semiconductor device according to claim 2,
wherein, assuming that a breakdown voltage is
represented by V_B (V), then t, V_B (V), B and A satisfy
25 a relationship below:

$$t < 2.53 \times 10^{-6} \times (A \times V_B)^{7/6} \text{ (cm)}.$$

6. A semiconductor device according to claim 3,

wherein, assuming that an impurity concentration of the first semiconductor layer is represented by N_n and that a breakdown voltage is represented by V_B (V), then N_n , V_B (V), and A satisfy the relationship below:

5
$$N_n > 1.11 \times 10^{18} \times (A \times V_B)^{-4/3} \text{ (cm}^{-3}\text{)}.$$

7. A semiconductor device according to claim 1, wherein an insulating material is interposed between the second semiconductor layer and the third semiconductor layer.

10 8. A semiconductor device according to claim 7, wherein a void is present in said insulating material.

9. A semiconductor device according to claim 1, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

15 10. A semiconductor device according to claim 2, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

20 11. A semiconductor device according to claim 3, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

25 12. A semiconductor device according to claim 4, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

13. A semiconductor device according to claim 5, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

5 14. A semiconductor device according to claim 6, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

10 15. A semiconductor device according to claim 7, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

15 16. A semiconductor device according to claim 8, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

20 17. A semiconductor device according to claim 1, wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer.

18. A semiconductor device according to claim 17, wherein a plurality of voids are present independently along the border region.

25 19. A semiconductor device according to claim 17, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

20. A semiconductor device according to claim 18, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.